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Michael Burns
MICHAEL BURNS

Docket No.: GR 99 P 1878

Date: June 8, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : JENOE TIHANYI ET AL.

Title : POWER SWITCH

2 sheets of formal drawings in triplicate.
A check in the amount of $ 690.00 covering the filing fee.
Information Disclosure Statement and 3 References.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

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LAG:kc

# POWER SWITCH

## Background of the Invention:

### Field of the Invention:

The present invention lies in the electronics and electrical engineering fields. More specifically, the invention relates to a power switch having the following features:

- a first transistor having a load path and a control electrode;
- a first limiting transistor for limiting a voltage drop across the load path of the first transistor, having a load path connected in series with the load path of the first transistor, and having a control electrode.

A power switch of this type is disclosed in U.S. Patent No. 5,285,369 to Balakrishnan (see European published patent application EP 0 585 788 A1). There, the first transistor is MOSFET whose load path (drain-source path) is connected in series with the load path of a junction field-effect transistor, also referred to as called junction FET (JFET). The source electrode of the MOSFET and the gate electrode of the JFET are in this case connected to a common node. The JFET is in the on state when the MOSFET is in the on state. If the

MOSFET is turned off when a corresponding potential is applied to its gate electrode, the JFET is initially still in the on state. The drain potential of the MOSFET and the source potential of the JFET rise until the gate-source voltage of the JFET reaches the value of the reverse voltage. The JFET turns off and thereby limits a further voltage rise across the load path of the MOSFET, in order to protect the latter against being destroyed by overvoltage.

In the prior art power switch, the value of the voltage obtained across the load path of the MOSFET is limited to the value of the reverse voltage of the JFET. The maximum permissible voltage which can be switched non-destructively through the power switch is given by the sum of the maximum load path voltages of the JFET and of the MOSFET.

Summary of the Invention:

It is accordingly an object of the invention to provide a power switch, which overcomes the disadvantages of the heretofore-known devices and methods of this general type.

With the foregoing and other objects in view there is provided, in accordance with the invention, a power switch, comprising:

a controllable transistor having a load path and a control electrode;

a limiting transistor for limiting a voltage drop across the load path of the first transistor, the limiting transistor having a load path connected in series with the load path of the first transistor, and having a control electrode; and

an auxiliary transistor having a load path connected between the control electrode of the limiting transistor and a reference node, and having a control electrode connected between the first transistor and the limiting transistor.

In contrast with the prior art, therefore, the power switch according to the invention has a first auxiliary transistor with a load path connected between the control electrode of the first limiting transistor and a reference node, and a control electrode connected between the first transistor and the first limiting transistor.

The auxiliary transistor of the power switch according to the invention, which is preferably a junction field-effect transistor of a complementary conductivity type with respect to the conductivity type of the limiting transistor, serves, when the first transistor is turned off, for setting a gate potential of the first limiting transistor which lies above

the potential of the reference node. As a result, until the limiting transistor is turned off, a higher voltage can be dropped across the load path of the first transistor than is prescribed by the reverse voltage of the limiting transistor according to the prior art. In order to limit the gate potential of the first limiting transistor, a Zener diode is advantageously connected in parallel with the load path of the first auxiliary transistor, which diode turns on when its breakdown voltage is reached.

In accordance with an added feature of the invention, at least one further limiting transistor has a load path connected in series with the load path of the first above-mentioned limiting transistor, and at least one further auxiliary transistor has a load path connected between the control electrode of the first-mentioned limiting transistor and the control electrode of the second limiting transistor, and a control electrode connected between the load paths of the first and further limiting transistors. Zener diodes are advantageously connected in parallel with the auxiliary transistors.

The addition of further limiting transistors whose load paths are each connected in series, and to whose control electrodes respective auxiliary transistors are connected for the purpose of setting a control electrode potential of the limiting

transistors, makes it possible advantageously to increase the maximum voltage that can be switched through the power switch, without risking the destruction of the first transistor and of the limiting transistors. In this case, the first transistor and the limiting transistors each accept a portion of the voltage dropped across the load path of the power switch, the first transistor and the limiting transistors preferably being dimensioned in such a way that they can accept only a portion of the maximum total voltage without being destroyed.



The distribution of the total voltage between a plurality of transistors has a beneficial effect on the resistance of the power switch in the on state. For transistors, it holds true that said resistance rises exponentially with the maximum permissible load path voltage for the transistor. If the number of series-connected transistors used is fixedly prescribed, then in the case of such a circuit in which the transistors are designed each to accept a specific portion of the total voltage, the resistance is exponentially dependent on the maximum permissible total voltage. By contrast, the invention makes it possible, independently of the maximum permissible total voltage of the power switch, always to use transistors having the same maximum load path voltage and to vary the number of series-connected transistors. The dielectric strength of the power switch rises with each transistor by a value prescribed by the dielectric strength of

the individual transistor. At the same time, the resistance of the power switch rises by a value prescribed by the resistance of the individual transistor. The resistance thus rises proportionally to the dielectric strength, not exponentially with respect thereto.

In accordance with an additional feature of the invention, the load path of the controlled transistor is connected between the limiting transistor and the reference node. In other words, that load path terminal of the first transistor which is remote from the first limiting transistor is connected to the reference node.

In accordance with another feature of the invention, a power switch control terminal is connected to the control electrode of the controllable transistor.

In accordance with a further feature of the invention, the limiting transistor has a source electrode and a gate electrode, and a Zener diode is connected between the source electrode and the gate electrode of the limiting transistor. In the cascaded switch embodiment, a Zener diode is connected between the source electrode and the gate electrode of each limiting transistor.

In accordance with again an additional feature of the invention, a Zener diode is connected in parallel with the load path of the auxiliary transistor. In the cascaded switch embodiment, Zener diodes are connected in parallel with the load paths of each of the auxiliary transistors.

In accordance with again a further feature of the invention, the controllable transistor is a MOSFET of a first conductivity type, the limiting transistor is a normally on field-effect transistor of the first conductivity type, and the auxiliary transistor is a normally on field-effect transistor of a second conductivity type. These variants are equally true in the multi-auxiliary transistor embodiment.

In accordance with yet a further feature of the invention, the controllable transistor, the limiting transistor, and the auxiliary transistor are integrated in a semiconductor body.

With the above and other objects in view there is provided, in accordance with the invention, a semiconductor body with a power switch formed in the semiconductor body and having a load path running vertically through the semiconductor body. The semiconductor body comprises:

a substrate doped with charge carriers of a first conductivity type;

at least one well doped with charge carriers of a second conductivity type, and a MOSFET formed in the at least one well;

a first region formed in the substrate spaced apart from the well and heavily doped with charge carriers of the first conductivity type; and

a second region horizontally spaced apart from the first region and heavily doped with charge carriers of a second conductivity type.

In accordance with yet again a further feature of the invention, the first region is one of a plurality of first regions formed in the semiconductor body and spaced apart from one another in the vertical direction, and the second region is one of a plurality of second regions formed in the semiconductor body and spaced apart from one another in the vertical direction.

In accordance with a concomitant feature of the invention, interconnects connect respectively adjacent second regions, the interconnects being formed by doping with charge carriers of the second conductivity type. The well is connected to the second region by an interconnect.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a power switch, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a schematic circuit diagram of a first embodiment of the power switch according to the invention;

Fig. 2 is a schematic circuit diagram of a second embodiment of the power switch according to a second embodiment of the invention; and

Fig. 3 sectional view through shows a semiconductor body in cross section with an integrated power switch according to the invention.

Unless indicated otherwise, identical reference symbols refer to functionally and structurally equivalent parts throughout the drawing figures.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is seen a circuit diagram of an exemplary embodiment of a power switch according to the invention.

The power switch is used to switch a voltage between a first connecting terminal AK1 and a second connecting terminal AK2. The switching is dependent on a control signal present at a control terminal SK.

The power switch has a first transistor T1, which is an n-conducting MOSFET in the exemplary embodiment, and a limiting transistor T2, which is an n-conducting junction FET in the exemplary embodiment. A load path of the MOSFET T1, which runs between the drain electrode D and the source electrode S of the latter, is connected in series with a load path of the junction FET T2, which runs between the drain electrode D and

the source electrode S of the latter, the drain terminal D of the MOSFET T1 being connected to the source terminal S of the junction FET T2. The gate electrode G of the MOSFET T1, which serves as switching element in the power switch, is connected to the control terminal SK of the power switch.

The limiting transistor T2 designed as a junction FET serves for limiting a voltage dropped across the load path D-S of the MOSFET T1 when the latter turns off. To that end, the junction FET T2 turns off when the drain potential of the MOSFET T1 exceeds a specific value.

In order to drive the limiting transistor T2, there is provided an auxiliary transistor T3 in the form of a p-conducting junction FET in the exemplary embodiment. The transistor T3 has a load path which runs between a source electrode S and a drain electrode D and is connected between the gate electrode G of the limiting transistor T2 and a reference node. In the exemplary embodiment, the reference node is formed by the second output terminal AK2, to which the source terminal S of the MOSFET T1 is also connected. The gate electrode G of the auxiliary transistor T3 is connected to a node which is common to the source electrode S of the limiting transistor T2 and to the drain electrode D of the MOSFET T1. The gate electrode G of the limiting transistor T2 and the source electrode S of the auxiliary transistor T3 are

connected to the first connecting terminal AK1 via a first Zener diode Z1. The gate potential of the limiting transistor T2 is limited by a further Zener diode Z3 which is connected in parallel with the load path of the first auxiliary transistor T3.

In order to illustrate the function of the power switch, in the exemplary embodiment according to Fig. 1 the power switch is connected between a reference potential M and a terminal of a load L by means of the connecting terminals AK1, AK2. The load L is connected to a supply potential V+ by means of a further terminal.

When a potential that is positive with respect to the reference potential M and that suffices to switch on the MOSFET T1 is present at the control terminal SK of the power switch, and hence at the gate electrode G of the MOSFET T1, the limiting transistor T2 (as a normally-on transistor, T2 is maximally in the on state when the gate-source voltage is zero, and its conductivity decreases toward negative gate-source voltage values) turns on and the p-conducting auxiliary transistor T3, whose conductivity decreases toward positive gate-source voltage values, turns on. The power switch is "closed". Approximately the entire supply voltage is then dropped across the load L, if the load L is large with respect

to the sum of the load path resistances of the MOSFET T1 and of the limiting transistor T2.

When the MOSFET T1 is turned off by reducing the potential at the control terminal SK, there is a rise in the potential at its drain electrode D and at the source electrode S of the limiting transistor T2 and the gate electrode G of the auxiliary transistor T3. The auxiliary transistor T3 starts to turn off. As a result, the gate potential of the limiting transistor T2 rises and the latter remains in the on state. The gate potential of the limiting transistor T2 and the voltage across the load path of the auxiliary transistor T3 rise until the breakdown voltage of the further Zener diode Z3 is reached and a further rise in potential is thereby prevented. With a further rise in the potential at its source electrode S, the limiting transistor T2 starts to turn off. When the gate-source voltage of the limiting transistor T2 reaches the value of the reverse voltage, the limiting transistor T2 turns off completely and thus prevents a further voltage rise across the load path of the MOSFET T1. The difference between the voltage that is present between the connecting terminals AK1, AK2 and the voltage dropped across the load path of the MOSFET T1 is accepted by the limiting transistor T2, which is dimensioned accordingly.

Referring now to Fig. 2, there is shown a further exemplary embodiment of a power switch according to the invention. The second embodiment differs from the first embodiment of Fig. 1 by the fact that further limiting transistors T4, T6 are connected in series with the limiting transistor T2. In order to set the gate potentials of the second and third limiting transistors T4, T6, a second and third auxiliary transistor T5, T7 are provided, the load path of the second auxiliary transistor T5 being connected up between the gate electrodes G of the first limiting transistor T2 and of the second limiting transistor T4, and the load path of the third auxiliary transistor T7 being connected up between the gate electrodes G of the second limiting transistor T4 and of the third limiting transistor T6. Further Zener diodes Z5, Z7 are respectively connected in parallel with the load paths of the second and third auxiliary transistors T5, T7. The source electrode of the auxiliary transistor T7 is connected to the first connecting terminal AK1 via the first Zener diode Z1.

The dielectric strength of the power switch can be increased by cascading further limiting transistors T4, T6 and further auxiliary transistors T5, T7. When the MOSFET T1 turns off in the exemplary embodiment according to Fig. 2, the gate potential of the limiting transistor T2 rises until the breakdown voltage of the Zener diode Z3 is reached. The source potential of the limiting transistor T2 then also rises until

the gate-source reverse voltage is reached and the limiting transistor T2 turns off. As a result, the voltage across the load path of the limiting transistor T2 rises, and the source potential of the second limiting transistor T4 connected in series with said limiting transistor T2 rises. The associated auxiliary transistor T5 starts to turn off and allows the gate potential of the second auxiliary transistor T5 to rise until the breakdown voltage of the parallel-connected Zener diode Z5 is reached. The source potential of the second limiting transistor T4 then also rises until the latter's reverse voltage is reached and the limiting transistor T4 turns off and thereby prevents a further voltage rise across the load path of the limiting transistor T2. If the second limiting transistor T4 turns off, the source potential of the third limiting transistor T6 rises and, via the third auxiliary transistor T7, the latter's gate potential rises, until the breakdown voltage of the Zener diode Z7 is reached and, after a further rise in the source potential, the third limiting transistor T6 turns off and thus prevents a further rise in the load path voltage of the second limiting transistor T4. The difference in the voltage between a supply voltage V+ and the voltage already dropped across the load paths of the MOSFET T1 and of the limiting transistors T2, T4 is accepted by the third limiting transistor. The limiting transistors T2, T4, T6 turn off one after the other, proceeding from the first limiting transistor T2, in which case some of the limiting

transistors can also remain in the on state if the voltage present between the connecting terminals AK1, AK2 is already accepted by the other limiting transistors. The number of limiting transistors T2, T4, T6 to be connected in series can be chosen in a manner dependent on the voltage to be switched. As many limiting transistors T2, T4, T6 as desired can be connected in series, and can be driven by auxiliary transistors T3, T5, T7 connected up correspondingly.

The power switch according to the invention has been described in Figs. 1 and 2 using n-conducting transistors as limiting transistors and p-conducting transistors as auxiliary transistors. It goes without saying that it is also possible to use p-conducting transistors as limiting transistors and n-conducting transistors as auxiliary transistors, in which case it is then necessary to interchange the polarities of the Zener diodes.

Referring now to Fig. 3, there is shown a cross section through a detail of a semiconductor body 10, in which a power switch according to the invention is integrated. The semiconductor body 10 has a substrate 12, which is n-conducting in the exemplary embodiment. One or more heavily p-doped wells 14, 15 are introduced into the substrate from one side of the semiconductor body, in which wells, in turn, heavily n-doped wells 16, 17 are formed. The p-doped wells 14,

15 with the n-doped wells are each part of cells of a MOSFET T1 formed in the semiconductor body 10. The heavily n-doped wells 16, 17 constitute the source regions of the MOSFET T1, which can be contact-connected externally via a metalization layer or a polysilicon and form the first connecting terminal AK1 of the power switch. Arranged such that they are isolated from the semiconductor body 10 by an insulation layer are gate electrodes 18, 19, which extend in the horizontal direction in each case from the heavily n-doped wells 16, 17 as far as the n-doped substrate 12 and are connected together to form a gate terminal G. That region of the substrate 12 which surrounds the p-doped wells 14, 15 forms the drain region of the MOSFET T1.

The substrate 12 is heavily n-doped in a region 20, which is opposite to the surface at which the MOSFET T1 is formed. This region forms the first connecting terminal AK1 of the power switch.

In the illustrated example, heavily p-doped regions 32, 34, 36 are arranged successively in the vertical direction between the cells of the MOSFET T1 and the region 20, respectively adjacent regions 32, 34; 34, 36 and the region 32 and the p-doped well 14 being connected to one another by weakly p-doped tracks 33, 35, 37. Heavily n-doped regions 42, 44, 46 are arranged such that they are spaced apart from the p-doped

regions 32, 34, 36 in the horizontal direction, and are arranged such that they are respectively adjacent to one another in the vertical direction. There is a corresponding structure situated above the well 15, the structure only being partially illustrated, and without reference symbols. A multiplicity of such structures are preferably formed in the semiconductor body 10.

Such a structure may be fabricated e.g. by multilayer epitaxial deposition with ion implantation on the intermediate surfaces and outdiffusion from the implanted regions. The heavily p-doped regions 32, 34, 36, the heavily n-doped regions 42, 44, 46 and the p-doped tracks 33, 35, 37 may be diffused zones with non-uniform doping. The substrate 12 need not be doped uniformly either.

The p-doped regions 32, 34, 36 and the n-doped regions 42, 44, 46 form limiting transistors T2, T4, T6 and auxiliary transistors T3, T5, T7 with parallel Zener diodes Z3, Z5, Z7 with the circuitry connections illustrated in Fig. 2. In order to provide a better understanding, the circuit symbols of the limiting transistors T2, T4, T6, of the auxiliary transistors T3, T5, T7 and of the Zener diodes Z3, Z5, Z7 are portrayed by broken lines with the corresponding reference symbols in Fig. 3. As is illustrated in Fig. 3, the heavily p-doped regions 32, 34, 36 constitute the drain and source regions of the

auxiliary transistors T3, T5, T7, the gate regions of the limiting transistors T3, T5, T7 and the anode and cathode regions of the Zener diodes Z3, Z5, Z7. Furthermore, the heavily n-doped well 14 forms the drain region of the auxiliary transistor T3.

The heavily n-doped regions 42, 44, 46 form the drain and source regions of the limiting transistors T2, T4, T6 and the gate regions of the limiting transistors T3, T5, T7.

If, in order to "close" the switch, a positive voltage is applied between the gate electrode G and the source electrode S of the MOSFET T1, a conduction region forms in the heavily p-doped wells 14, 15 and, in the event of a voltage being applied between the first and second connecting terminals AK1, AK2, a current flows from the first connecting terminal AK1 via the region 20, the substrate 12, the p-doped well 14 and the n-doped well 16 to the second connecting terminal AK2.

If the MOSFET T1 turns off, for example as a result of short-circuiting of the gate and source electrodes G, S with voltage present between the connecting terminals AK1, AK2, a space charge zone starts to build up in the substrate 12 proceeding from the MOSFET T1. If the space charge zone reaches the p-doped regions 32, 34, 36 in succession, positive potentials are established there, as a result of which charge carriers

are bound around the p-doped regions 32, 34, 36 and, in particular, current can no longer flow between the heavily n-doped regions 42, 44, 46. The power switch turns off.

We claim:

1. A power switch, comprising:

a controllable transistor having a load path and a control electrode;

a limiting transistor for limiting a voltage drop across said load path of said first transistor, said limiting transistor having a load path connected in series with said load path of said first transistor, and having a control electrode; and

an auxiliary transistor having a load path connected between said control electrode of said limiting transistor and a reference node, and having a control electrode connected between said first transistor and said limiting transistor.

2. The power switch according to claim 1, wherein said limiting transistor is a first limiting transistor and said auxiliary transistor is a first auxiliary transistor, and at least one second limiting transistor has a load path connected in series with said load path of said first limiting transistor, and at least one second auxiliary transistor has a load path connected between said control electrode of said first limiting transistor and said control electrode of said second limiting transistor, and a control electrode connected

between said load paths of said first and second limiting transistors.

3. The power switch according to claim 1, wherein said load path of said controlled transistor is connected between said limiting transistor and said reference node.

4. The power switch according to claim 1, which further comprises a power switch control terminal connected to said control electrode of said controllable transistor.

5. The power switch according to claim 1, wherein said limiting transistor has a source electrode and a gate electrode, and a Zener diode is connected between said source electrode and said gate electrode of said limiting transistor.

6. The power switch according to claim 2, wherein each of said first and at least one second limiting transistors has a source electrode and a gate electrode, and a Zener diode is connected between said source electrode and said gate electrode of each said limiting transistor.

7. The power switch according to claim 1, which comprises a Zener diode connected in parallel with said load path of said auxiliary transistor.

8. The power switch according to claim 2, which comprises Zener diodes connected in parallel with said load paths of each said auxiliary transistor.

9. The power switch according to claim 1, wherein said controllable transistor is a MOSFET of a first conductivity type, said limiting transistor is a normally on field-effect transistor of the first conductivity type, and said auxiliary transistor is a normally on field-effect transistor of a second conductivity type.

10. The power switch according to claim 2, wherein said controllable transistor is a MOSFET of a first conductivity type, said first and second limiting transistors are normally on field-effect transistors of the first conductivity type, and said first and second auxiliary transistors are normally on field-effect transistors of a second conductivity type.

11. The power switch according to claim 1, wherein said controllable transistor, said limiting transistor, and said auxiliary transistor are integrated in a semiconductor body.

12. The power switch according to claim 1, wherein said controllable transistor, said first and second limiting transistors, and said first and second auxiliary transistors are integrated in a semiconductor body.

13. A semiconductor configuration, comprising:

a semiconductor body and a power switch formed in said semiconductor body and having a load path running vertically through said semiconductor body;

said semiconductor body being formed with:

a substrate doped with charge carriers of a first conductivity type;

at least one well doped with charge carriers of a second conductivity type, and a MOSFET formed in said at least one well;

a first region formed in said substrate spaced apart from said well and heavily doped with charge carriers of the first conductivity type; and

a second region horizontally spaced apart from said first region and heavily doped with charge carriers of a second conductivity type.

14. The semiconductor body according to claim 13, wherein said first region is one of a plurality of first regions formed in said semiconductor body and spaced apart from one another in the vertical direction, and said second region is

one of a plurality of second regions formed in said semiconductor body and spaced apart from one another in the vertical direction.

15. The semiconductor body according to claim 14, which comprises interconnects connecting respectively adjacent second regions, said interconnects being formed by doping with charge carriers of the second conductivity type, and wherein said well is connected to one of said second regions by an interconnect.

Abstract of the Disclosure:

The power switch has a first transistor, a limiting transistor, and an auxiliary transistor. The first transistor has a load path and a control electrode. The limiting transistor, which limits a voltage drop across the load path of the first transistor, has a load path connected in series with the load path of the first transistor, and a control electrode. The auxiliary transistor has a load path connected between the control electrode of the limiting transistor and a reference node, and having a control electrode connected between the first transistor and the limiting transistor.



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FIG 1

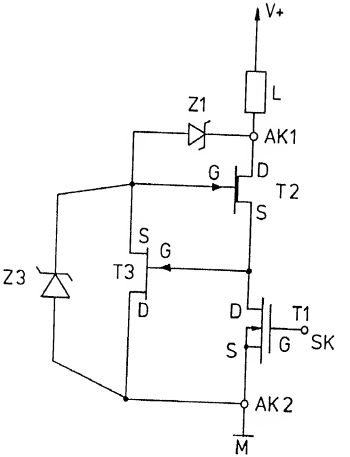



FIG 2

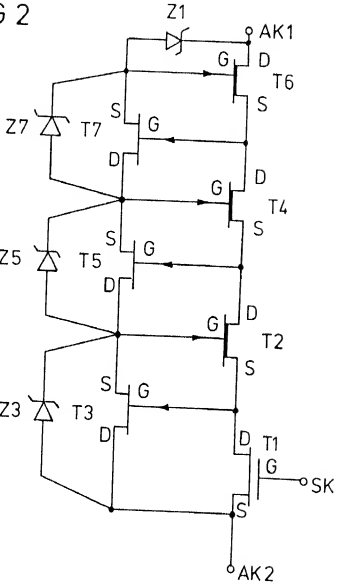
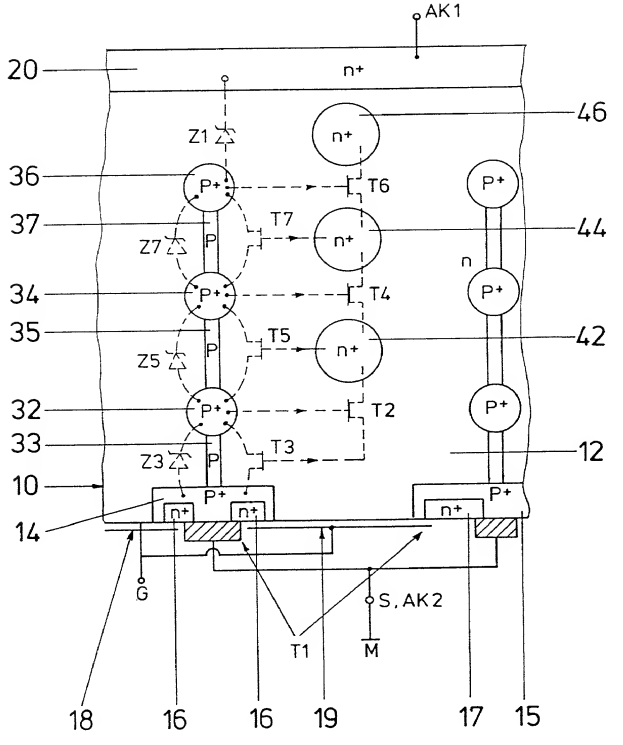


FIG 3


AK1
20
n+
46
Z1
36
P+
T6
37
T7
44
Z7
P
n
34
T4
35
T5
42
Z5
32
T2
33
T3
12
Z3
10
14
G
S, AK2
T1
M
18
16
16
19
17
15

Docket No.: GR 99 P 1878

**COMBINED DECLARATION AND POWER OF ATTORNEY IN ORIGINAL APPLICATION**

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

POWER SWITCH

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 199 26 109.1, filed June 8, 1999, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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